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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,173	08/25/2000	Rajeev Jayavant	P04211	6232

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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2676	17

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/648,173	JAYAVANT ET AL.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Remarks

1. This Office Action is in response to applicant's response dated July 14, 2004 in response to PTO Office Action dated February 11, 2004. The amendments to claim(s) 1, 7, 14, 20 and 26; addition of new claims 27-30 have been entered into the record and applicant's remarks have been carefully considered resulting in the action as set forth herein below.

2. Applicant's arguments filed November 10, 2003 with respect to amended claim(s) 1, 7, 14, 20 and 26 and the new claims 27-30 have been considered but are not persuasive.

3. With respect to applicant's argument to claim 1, the amended claim introduces claim limitations "...plurality of stages including a first stage and a last stage and intermediate stages of the pipelines pertaining to 2-D and 3-D pipelines...", DiNicola et al. **discloses** processing nodes including a first processor, a second processor which are serially coupled to each other thus providing plurality of stages with first stage, last stage and an intermediate stage (col. 6, lines 52-65).

4. With respect to applicant's argument to claim 1 that image processing system uses common circuitry at an intermediate stage that can be selectively placed in one mode or another, such claim limitation is absent from claim 1 language. DiNicola et al. **discloses** dual pipelines for 2-D and 3-D processing.

5. With respect to applicant's argument to claim 1 that DiNicola-Ezer combination differs from the invention in that dual-mode sub-processing circuitry performs graphics processing on data that already has been processed in, DiNicola **discloses** interleaved 2D and 3D graphics data being received via bus interface 302 (col. 5, lines 34-61)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,394,524 to DiNicola et al. in view of U.S. Patent No. 6,275,239 B1 to Ezer et al., and further in view of U.S. Patent No. 6,208,350 B1 to Herrera.

a. Regarding claims 1 and 7, DiNicola et al. **discloses** an image processing circuitry (graphics subsystem 300, control processing unit 328, RAM 330, Raster subsystem 326), comprising: a two-dimensional image pipeline (2D subsystem 301) with plurality of stages that is operable to process two dimensional image data (incoming 2D data stream) to generate successive two dimensional image frames for display in a two-dimensional image space; a three-dimensional image pipeline (3D processing node 305) with plurality of stages that is operable to process three-dimensional image data to render successive three dimensional image frames for display in a two-dimensional image space; and dual mode sub-processing circuitry (attribute processor (AP) 306), associated with each of said two-dimensional image pipeline (2D subsystem 301) and said three-dimensional image pipeline (3D processing node 305), to perform rasterization operations (...reordering device 322 combines the processed 3D data from the processing nodes 305 into a single 3D data stream for transmission to the raster subsystem 326...col. 7, lines 27-29) associated said three-dimensional image pipeline in another mode. DiNicola et al. **suggests** a graphics subsystem comprising a two-dimensional image pipeline that is operable to perform processing the two dimensional image data

(...the ...2D subsystem...provides ...processing for a 2D...data stream...col. 3, lines 37-40) in one mode. However, DiNocala et al. **is silent about** wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs operations associated with said two-dimensional image pipeline and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs operations associated with said three-dimensional image pipeline. Ezer et al. **discloses** a media coprocessor 102 which supports 3-D graphics, video and audio (...medio coprocessor 102 provides an application spectrum including: 3D textured, shaded, z-buffered, antialiased, blended polygons; 2D scaled, rotated, and translated transparent sprite image...col. 3, lines 1-26). The media processor 102 performs different operations using its several functional units such as :digital signal processor 202 that performs 2D and 3D functions (col. 4, lines 1-16) thus **disclosing** similarity in circuit implementation that allows common circuitry to share functions associated with two- and three-dimensional image pipelines and the seemingly different operations required thereby which is similarly recited in the instant claim. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the "(attribute processor (AP) 306)" with the feature "a media coprocessor that is able to provide an application spectrum including: 3D textured, shaded, z-buffered, antialiased, blended polygons; 2D scaled, rotated, and translated transparent sprite image; geometry processing for 2D and 3D graphics; data-driven display pipeline supporting both geometric 3-D graphics and image data types" as taught by Ezer et al. **because** it results in improved cost/performance to applications. However, DiNicola et al. **does not suggest** graphics operations associated with said two-dimensional image pipeline (2D subsystem 301) in one mode. Herrera **discloses** a method for generating graphics and processing digital video signals in a computer system using a graphics engine to generate

digital image data based on at least one command signal similar to "one mode or another" as per the instant claim and the same graphics engine generating motion compensated digital image data based on at least one digital image map and at least one motion vector (col. 5, lines 5-67; col. 6, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by DiNicola-Ezer combination with the feature "mode selection based on a command signal" as taught by Herrera **because** it provides a cost-effective solution for doing both 2D and 3D processing in one system (col. 6, lines 1-11; col. 13, lines 66-67; col. 14, lines 1-6).

b. Regarding claims 2 and 8, DiNicola-Ezer combination **implicitly discloses** a portion of dual mode sub-processing circuitry (attribute processor (AP) 306) to perform texture mapping in said another mode. However, DiNicola-Ezer combination **does not suggest explicitly** to perform texture mapping in said another mode and to sample reference frames in said one mode. Herrera **discloses** both the texture mapping and the sampling of reference frames based on mode of operation (...based on at least one command signal...col. 6, lines 2-3)(...the apparatus includes a setup-engine...a texture mapping engine...bilinear interpolator...determines interpolated digital pixel data based on a first and a second digital pixel data...and averages the results of the first...filtering...to generate...predicted macroblock...col. 5, lines 5-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the DiNicola-Ezer combination with the feature "sampling reference frames and texture mapping" as taught by Herrera **because** there are similarities between the process of motion compensation, which includes sampling reference frames and texture mapping, which is a part of three-dimension graphics data processing, thus

providing a cost-effective solution for doing both in one system (col. 13, lines 66-67; col. 14, lines 1-6).

c. Regarding claims 3 and 9, DiNicola et al. as modified by Ezer et al. **discloses** blending samples from a plurality of reference frames in said one mode and to blend samples from a plurality of texture maps in said another mode (...for 3D graphics ...performs...texture resampling...blending...col. 11, lines 1-22).

d. Regarding claims 4 and 10, DiNicola-Ezer combination **is silent about** processing said plurality of reference frames using error term in said one mode and to perform alpha blending in said another mode. Herrera **discloses** processing said plurality of reference frames using error term in said one mode (...a typical 3D graphics engine 92 is not configured ...to add a macroblock coefficient...thus in accordance... "8-bit signed addition ROP" is provided ...to handle the signed addition...col. 14, lines 66-67; col. 15, lines 1-19) and to perform alpha blending in said another mode (...frame buffer 56 is depicted as being subdivided into ..."on screen"..."off screen".... contains intermediate data, such as various texture maps 124a-n...to create/modify the current image...col. 12, lines 60-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by DiNicola-Ezer combination with the feature "to process plurality of reference frames using error terms and to perform alpha blending in said another mode" as taught by Herrera because it provides for a cost effective implementation of processing of reference frames using error terms and alpha blending in one system (col. 15, lines 1-32).

e. Regarding claims 5-6, 11-12, DiNicola-Ezer combination is **silent about** wherein 8- and 9-bit signed values are considered in context of MPEG processing. However, Herrera **teaches** a system able to support at least one MPEG standard (col. 5, lines 24-44) and an alpha blend sub-circuitry that is able to process at least 8- and 9-bit signed

values (col. 13, lines 24-67; col. 14, lines 1-67; col. 15, lines 1-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to modify the device as taught by DiNicola-Ezer combination with the feature "to process MPEG data and alpha blend sub-circuitry able to process 8- and 9-bit signed values" as taught by Herrera **because** it provides for a cost effective implementation of processing of reference frames using error terms and alpha blending in one system (col. 15, lines 1-32).

f. Regarding claim 13, DiNicola-Ezer combination **teaches** the method of operating said dual mode sub-processing circuitry (attribute processor (AP) 306) comprising the step of controlling said dual mode sub-processing circuitry (attribute processor (AP) 306) (...an attribute processor (AP) 306 performs preprocessing...and dispatches work to the 3D.. nodes or to the 2D subsystem...as appropriate...col. 5, lines 55-61).

g. Regarding claim 14, it is similar in scope to claim 13 above and is rejected under the same rationale.

h. Regarding claim 15, it is similar in scope to claim 13 and 8 above and is rejected under the same rationale.

i. Regarding claim 16, it is similar in scope to claim 13 and 9 above and is rejected under the same rationale.

j. Regarding claim 17, it is similar in scope to claim 13 and 10 above and is rejected under the same rationale.

k. Regarding claim 18, it is similar in scope to claim 13 and 11 above and is rejected under the same rationale.

l. Regarding claim 19, it is similar in scope to claim 13 and 12 above and is rejected under the same rationale.

m. Regarding claim 20, it is similar in scope to claim 13 above and is rejected under the same rationale.

n. Regarding claim 21, it is similar in scope to claim 15 above and is rejected under the same rationale.

o. Regarding claim 22, it is similar in scope to claim 16 above and is rejected under the same rationale.

p. Regarding claim 23, it is similar in scope to claim 17 above and is rejected under the same rationale.

q. Regarding claim 24, it is similar in scope to claim 18 above and is rejected under the same rationale.

r. Regarding claim 25, it is similar in scope to claim 19 above and is rejected under the same rationale.

s. Regarding claim 26, it is similar in scope to claim 1 above and is rejected under the same rationale.

t. Regarding claim 27, it is similar in scope to claim 1 above and is rejected under the same rationale.

u. Regarding claim 28 and 29, DiNicola et al. **discloses** 2-D and 3-D pipelines to process two dimensional and three dimensional image data (col. 5, lines 33-61).

v. Regarding claim 30, DiNicola as modified by Ezer et al. **discloses** a media coprocessor 102 which supports 3-D graphics, video and audio (...media coprocessor 102 provides an application spectrum including: 3D textured, shaded, z-buffered, antialiased, blended polygons; 2D scaled, rotated, and translated transparent sprite image...col. 3,

lines 1-26). The media processor 102 performs different operations using its several functional units such as :digital signal processor 202 that performs 2D and 3D functions (col. 4, lines 1-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the "(attribute processor (AP) 306)" with the feature "a media coprocessor that is able to provide an application spectrum including: 3D textured, shaded, z-buffered, antialiased, blended polygons; 2D scaled, rotated, and translated transparent sprite image; geometry processing for 2D and 3D graphics; data-driven display pipeline supporting both geometric 3-D graphics and image data types" as taught by Ezer et al. **because** it results in improved cost/performance to applications.

Conclusion

8. Applicant's arguments have been considered but are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office at telephone number :(703)-306-0377.

dks

October 1, 2004

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600